AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) An encoder comprising:

a changing-point counter for counting changing points of n-bit data(n: a positive integer) to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit ~~which is true~~ that has a first value when the counting result exceeds a predetermined value;

a code converter for converting the n-bit data in such a way that bits of the n-bit data located at predetermined positions are inverted when the discrimination bit ~~is true~~ has the first value; and

a parallel-to-serial converter for converting (n + 1)-bit data to a (n + 1)-bit serial code, the (n + 1)-bit data being generated by adding the discrimination bit to an output of the code converter,

wherein the changing-point counter conducts its counting operation for (n + 1)-bit data generated by including a last bit of an immediately preceding n-bit serial code the encoder has dealt to the n-bit serial data.

2. (original) The encoder according to claim 1, wherein the discrimination bit is added to the (n + 1)-bit data as its first or last bit.

3-4. (canceled)

5. (currently amended) The encoder according to claim 2, wherein the n-bit serial data has an odd bit number and the discrimination bit is added to the (n +1)-bit serial code as its last bit;

and wherein when a last bit of the n-bit serial data is not a bit for conversion of the code converter, the counting result is equal to the predetermined value, and the last bit of the n-bit serial data ~~is true~~ has the first value, the discrimination bit is set to ~~be true~~ the first value.

6. (original) The encoder according to claim 1, wherein the predetermined value is a largest integer equal to or less than (1/2) x (a bit number of the n-bit serial data - 1).

7-18. (canceled)

19. (currently amended) A data transfer system comprising:

(a) a changing-point counter and a code converter located in a data transmission side;

the changing-point counter counting changing points of n-bit data (n: a positive integer) to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit ~~which is true~~ that has a first value when the counting result exceeds a predetermined value;

the code converter converting the n-bit data in such a way that bits of the n-bit data located at predetermined positions are inverted when the discrimination bit ~~is true~~ has the first value, thereby generating an inverted n-bit data; and

the code converter outputting a (n + 1)-bit serial code generated by adding the discrimination bit to the inverted n-bit data,

wherein the changing-point counter conducts its counting operation for (n + 1)-bit serial code generated by including a last bit of an immediately preceding (n + 1)-bit serial code the data transmission side has dealt to the n-bits of the (n + 1)-bit serial code;

(b) a code deconverter located in a data reception side;

the code deconverter deconverting the (n + 1)-bit serial code outputted from the code converter in such a way that some of the n-bits of the (n + 1)-bit serial code located at predetermined positions excluding the discrimination bit are inverted when the discrimination bit ~~is true~~ has the first value;

wherein the (n + 1)-bit serial code is serially transferred from the data transmission side to the data reception side.

20. (original) The system according to claim 19, wherein the discrimination bit is added to the (n + 1)-bit serial code as its first or last bit.

21-22. (canceled)

23. (currently amended) The system according to claim 19, wherein the n-bits of the (n + 1)-bit serial code excluding the discrimination bit is odd;

and wherein the discrimination bit is added to the (n + 1)-bit serial code as its last bit;

and wherein when a last one of the n-bits of the (n + 1)-bit serial code is not a bit for conversion of the code converter, the counting result is equal to the predetermined value, and the last one of the n-bits of the (n + 1)-bit serial code ~~is true~~ has the first value, the discrimination bit is set to ~~be true~~ the first value.

24. (original) The system according to claim 19, wherein the predetermined value is a largest integer equal to or less than (1/2) x (a bit number of the n-bit serial data - 1).

25. (new) An encoder comprising:

a changing-point counter for counting changing points of n-bit data(n: a positive integer) to generate a counting result, where values of adjoining bits change at each of the changing points, the changing-point counter outputting a discrimination bit that has a first value when the counting result exceeds a predetermined value;

a delay circuit that receives the discrimination bit and outputs a delayed discrimination bit;

a code converter for converting the n-bit data in such a way that bits of the n-bit data located at predetermined positions are inverted when the delayed discrimination bit has the first value; and

a parallel-to-serial converter for converting (n + 1)-bit data to a (n + 1)-bit serial code, the (n + 1)-bit data being generated by adding the delayed discrimination bit to an output of the code converter,

wherein the changing-point counter conducts its counting operation for (n + 1)-bit data generated by including a last bit of an immediately preceding n-bit serial code the encoder has dealt to the n-bit serial data.